UMP2

USB to 8-bit parallel FIFO
interface module

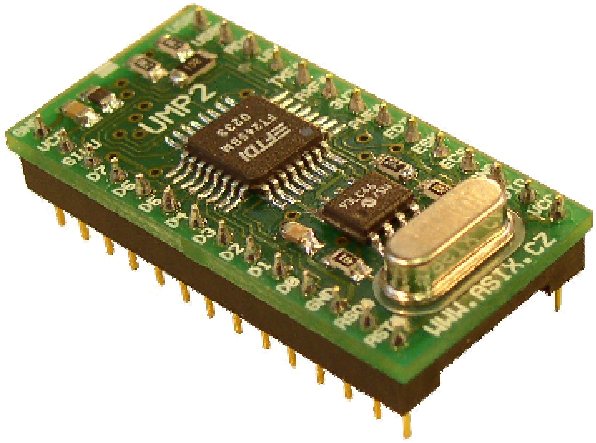
User’s manual

ASIX®

CONTENTS

1. UMP2

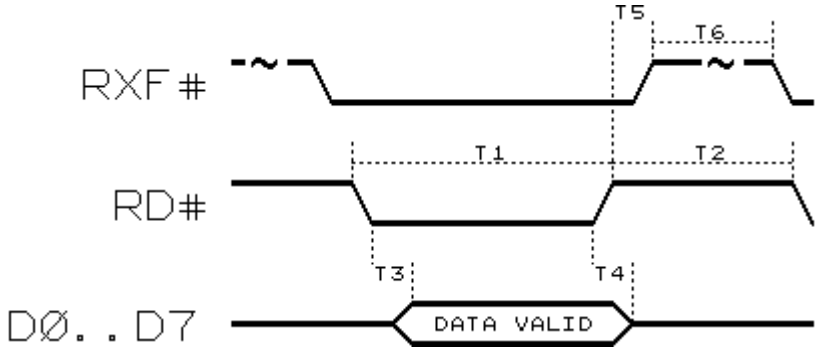
UMS2 is a module based on FT8U245BM integrated circuit manufactured by FTDI Ltd., which provides with easy to use USB connectivity to PC without any need of additional knowledge about USB itself.



2. USAGE

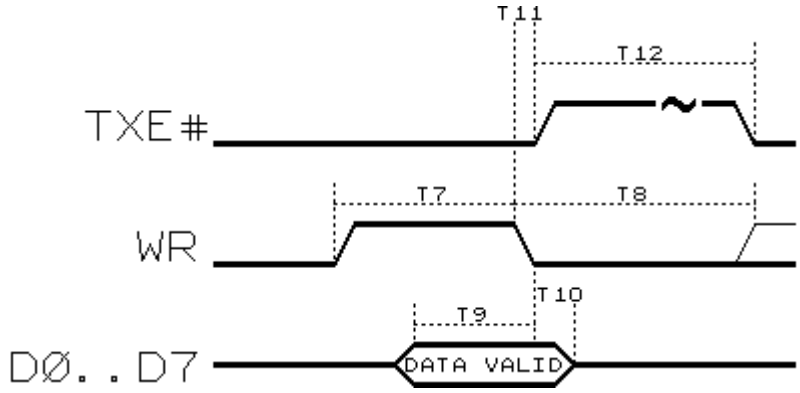
UMP2 is a USB to 8-bit bidirectional parallel FIFO interface with simple flow control.

2.1. FIFO read cycle



		min. [ns]	max. [ns]
T1	RD Active Pulse Width	50	
T2	RD to RD Pre-Charge Time	50	
T3	RD Active to Valid Data		30
T4	Valid Data Hold Time from RD inactive	10	
T5	RD Inactive to RXF#	5	25
T6	RXF# inactive after RD cycle	80	

2.2. FIFO write cycle



		min. [ns]	max. [ns]
T7	WR Active Pulse Width	50	
T8	WR to WR Pre-Charge Time	50	
T9	Data Setup Time before WR inactive		20
T10	Data Hold Time from WR inactive	10	
T11	WR inactive to TXE#	5	25
T12	TXE# inactive after WR cycle	80	

The module is capable of data transfer rates up to 1 MB/sec using direct driver and up to 3 MBd using virtual COM port driver. In addition there is an EEPROM memory which may be used to store VID and PID identifiers for OEM applications.

The module connects by 2 signals directly to USB connector, while the application side provides 8 bidirectional signals plus flow control.

From mechanical standpoint, the module is arranged as DIP28 with standard pin spacing of 0.1 inch (2.54 mm) so it is possible to fit it into either common or precise DIP28 socket, or to solder it directly to printed circuit board. The USB connector is to be connected externally which allows the designer to choose the placement of the connector and its type: 'B' or 'mini B' or USB cable soldered directly to the board may be used. This design sigificantly simplifies the development in small production series.

There is a separate power supply for IO pins (VCCIO), which allows the module to be connected to 3.0 V application easily.

The data transfer can be optimized by SI/WU signal which controls two functions: In suspend mode (PWREN#=1), if there is "Remote WakeUp" option in EEPROM turned on, falling edge will wake up the device. In normal operation, falling edge will force immediate data transfer to PC regardless of the amount of data in the buffer, otherwise the data is typically being sent in 64 byte blocks.

PWREN# signal is designated to drive a P-channel MOSFET for applications which drain more than 100 mA (max. 500 mA) from USB. In such case it is advisable to turn on 'enable pull-down' option in EEPROM configuration.

Module UMS2 can also operate in "BitBang mode", in which the data pins act as 8-bit parallel input/output. This mode can be used for example to configure programmable logic array directly from PC over USB.

Further, there is RSTOUT# signal, which stays in high impedance state for about 2 ms after power up and then it is connected to internal 3.3 V voltage regulator. Signal RSTOUT# is also in high inpedance state whenever signal RESET# is active (RESET#=log.0), but it is not affected by reset from USB (USB Bus RESET).

The module is equipped with 93LC56 memory of 128×16 bits. Lower half of this memory is used for module's needs (64×16 bits). Using EEDATA, EESK and EECS the application may use upper 64×16 bits for its own purposes. While the application is accessing module's EEPROM memory, the RESET# signal must be active (RESET#=log.0).

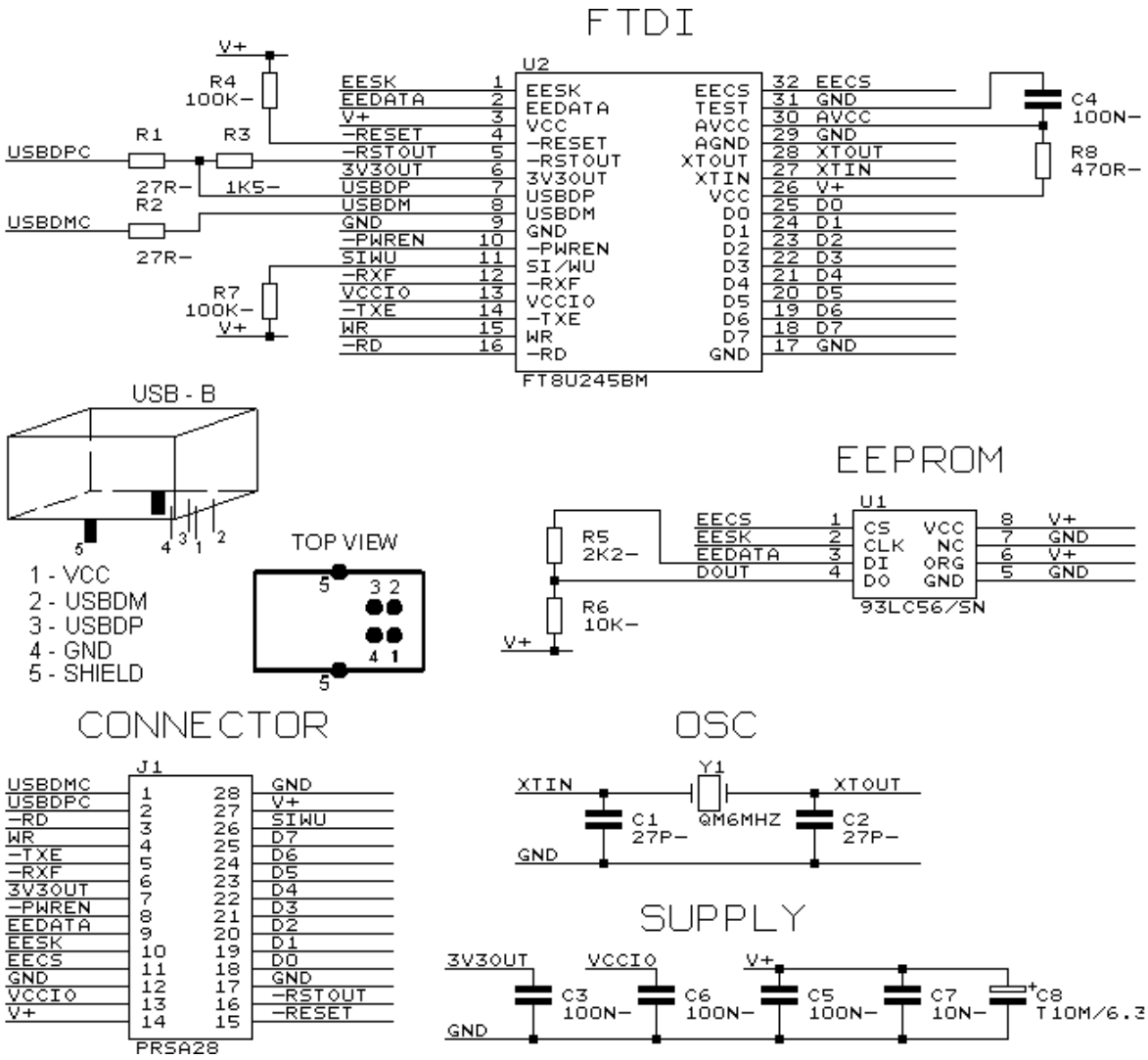
Software drivers fow Windows 98/ME/2K/XP, Mac OS8/OS9/OS X and Linux are available for free on FTDI website (http://www.ftdichip.com).

3. FEATURES

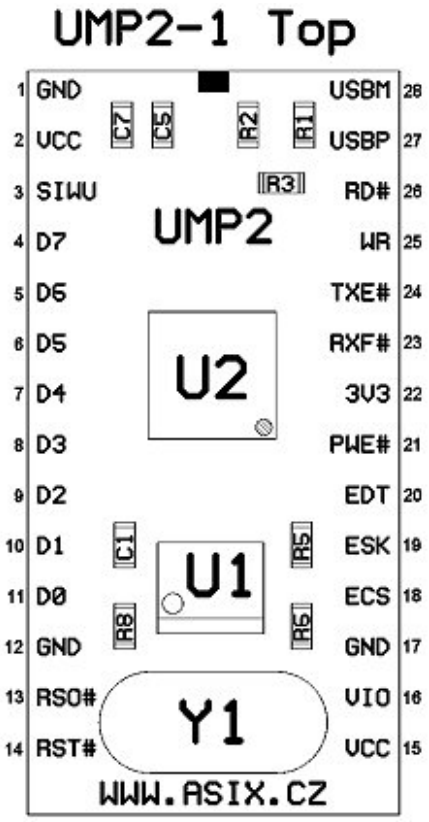
- Data inputs/outputs 3.0 to 5 V - CMOS compatible
- Powered from USB or external supply
- Data transfer rates up to 1 MB/sec with direct driver and up to 3 MBd with virtual COM port driver
- Hardware flow control
- 384 byte receive buffer
- 128 byte transmit buffer
- Supports USB 1.1 protocol, USB 2.0 compatible
- BitBang mode, which allows the module to be used as 8-bit bidirectional I/O (signals RD/WR/TXE#/RXF# are not used in this mode)
- PWREN# signal for driving P-channel MOSFET for applications draining more than 100 mA from USB (max. 500 mA)
- Support for OEM application (VID and PID are stored in EEPROM memory which is part of the module)
- Ability to use use free EEPROM capacity (64×16 bits)
- Drivers for Windows 98/2K/ME/XP, Mac OS8/OS9/OS X and Linux available for free
- DIP28 socket compatible, PCB mountable

4. TECHNICAL REFERENCE

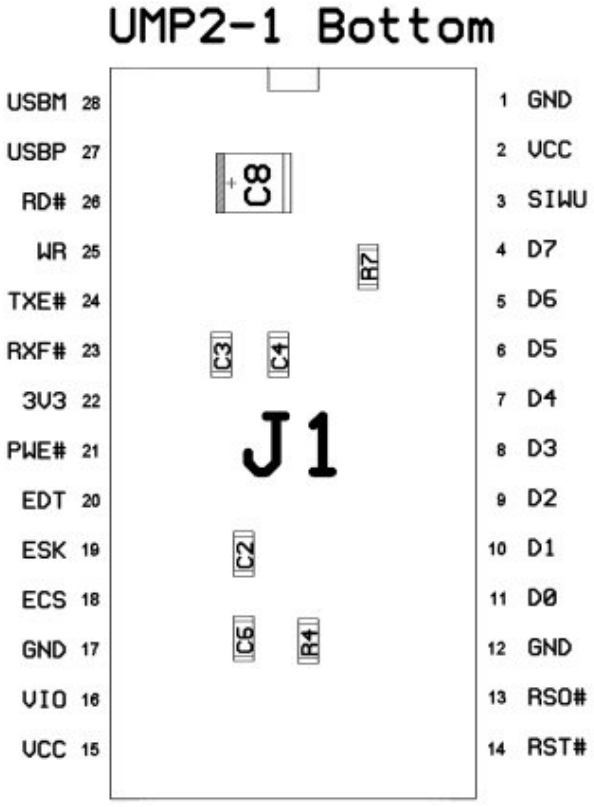
4.1. SCHEMATICS



4.2. TOP VIEW



4.3. BOTTOM VIEW



4.4. PIN DESCRIPTION

Pin	Label	FTDI	Typ	Description
1	GND	GND	PWR	Signal ground
2	VCC	VCC	PWR	Power supply +4.4 V to 5.25 V
3	SIWU	SI/WU	IN	Send immediate/WakeUp
4	D7	D7	I/O	Bidirectional data bus, bit 7
5	D6	D6	I/O	Bidirectional data bus, bit 6
6	D5	D5	I/O	Bidirectional data bus, bit 5
7	D4	D4	I/O	Bidirectional data bus, bit 4
8	D3	D3	I/O	Bidirectional data bus, bit 3
9	D2	D2	I/O	Bidirectional data bus, bit 2
10	D1	D1	I/O	Bidirectional data bus, bit 1
11	D0	D0	I/O	Bidirectional data bus, bit 0
12	GND	GND	PWR	Signal ground
13	RSO#	RSTOUT#	OUT	High impedance for about 2 ms after power up and during #RESET is active, otherwise connected to output of internal 3.3 V voltage regulator. This signal is not affected by USB Bus Reset.
14	RST#	RESET#	IN	External reset. May be left unconnected if not used.
15	VCC	VCC	PWR	Power supply +4.4 V to 5.25 V.
16	VIO	VCCIO	PWR	Power supply +3.0 V to +5.25 V for output drivers of pins 10..12, 14..16, 18..25.
17	GND	GND	PWR	Signal ground
18	ECS	EECS	I/O	EEPROM enable – internal pull-up of 200 kOhm during reset.
19	ESK	EESK	OUT	EEPROM clock - high impedance during reset.
20	EDT	EEDATA	I/O	EEPROM data I/O - high impedance during reset.
21	PWRE#	PWREN#	OUT	PWREN# - switched to log.0 after the module is configured and held in log.1 during reset and sleep mode (USB suspend). This signal may be used to drive P-channel MOSFET, which allows to connect applications draining more than 100 mA from USB.
22	3V3	3V3OUT	OUT	3.3 V output from internal voltage regulator - this pin can source up to 5 mA.
23	RXF#	RXF#	OUT	Data ready, if this signal is log.0, the data may be read by 1-0-1 sequence on RD# pin. If the RXF# signal is log.1, the data is invalid.

24	TXE#	TXE#	IN	Transmit enabled, if this signal is log.0 the data may be written by 0-1-0 sequence on WR pin. If the TXE# signal is log.1, the buffer if full.
25	WR	WR	IN	Write signal – falling edge of this signal writes data to FTDI buffer.
26	RD#	RD#	IN	Read data – falling edge of this signal causes 1 byte of data to be read from FTDI buffer and sent to data pins.
27	USBDP	USBDP	I/O	USB data signal plus. It is necessary to connect resistor of 1.5 kOhm between USBDP and 3V3OUT or RSTOUT#.
28	USBDM	USBDM	I/O	USB data signal minus.

5. DRIVER INSTALATION

For Windows operating systems there are two types of drivers:

- Virtual COM port, which can be accessed as common COM port using Win32 API
- Direct driver, to gain full control of the chip, a DLL to interface the driver is provided

Detailed description of driver installation procedure can be found on FTDI website (http://www.ftdichip.com).

6. TECHNICAL SPECIFICATION

6.1. ABSOLUTE RATINGS

Storage temperature	T_{STR}	min. -65 °C	max. 150 °C
Operational temperature	T_{PWR}	min. 0 °C	max. 70 °C
Power supply voltage	VCC_{MAX}	min. -0.5 V	max. 6.00 V
Input voltage – inputs	V_{IN1}	min. -0.5 V	max. VCC+0.5 V
Input voltage - I/O	V_{IN2}	min. -0.5 V	max. VCC+0.5 V
Output current – outputs	I_{O1}		max. 24 mA
Output current - I/O	I_{O2}		max. 24 mA
Power	W_{PWR}		max. 500 mW

6.2. TYPICAL RATINGS

VCC Operating supply voltage	VCC	min. 4.4 V	max. 5.25 V
Operating supply current	ICC_1		max. 50 mA
Suspended supply current	ICC_2		max. 250 µA
Input voltage log.1	V_{IH}	min. 2.0 V	
Input voltage log.0	V_{IL}		max. 1.0 V
Output voltage log.1	V_{OH}	min. 2.8 V, Ri=15 kOhm	
Output voltage log.0	V_{OL}		max. 0.3 V, Ri=1.5 kOhm
Output current log.1	I_{OH}	4 mA, VOH=VCC-0.5 V	
Input current log.0	I_{OL}	8 mA, VOL=0.5 V	

7. CONTACT

Address:	ASIX s.r.o., Staropramenna 4, 150 00 Prague, Czech Republic
Tel.:	+420-257 312 378
Fax:	+420-257 329 116
E-Mail:	info@pic-tools.com, support@pic-tools.com, sales@pic-tools.com
WWW:	www.pic-tools.com